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FAMOS—A NEW SEMICONDUCTOR CHARGE STORAGE DEVICE

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Abstract—A new non-volatile charge storage device is described. The floating gate avalanche injection MOS (FAMOS) structure is a *p*-channel silicon gate field effect transistor in which no electric contact is made to the silicon gate. It combines the floating gate concept with avalanche injection of electrons from the surface depletion region of a *p–n* junction to yield reproducible charging characteristics with long term storage retention.

INTRODUCTION

In recent years a growing interest has been expressed in nonvolatile semiconductor memories. This interest stems from the need for high density, low cost semiconductor memory chips as well as an attempt to provide a substitute for the nonvolatile storage capability (retention of stored information without an external power source) of magnetic memories. Initial research efforts in this direction have centered in the area of semiconductor Read Only Memories (ROM's). Most available semiconductor ROM's are programmed permanently at the integrated circuit fabrication stage by a custom mask which defines the desired information pattern. As a result, program changes involve the generation of a new mechanical mask for every modified ROM pattern. In addition to being an expensive step, it also limits the flexibility of ROM applications because of the delay involved in the production process. Substitution of the delay in the generation and processing of a custom mask provides an ideal application area for nonvolatile semiconductor storage devices, since it does not impose a stringent requirement on the speed of electrical programming.

Most proposed non-volatile semiconductor storage devices rely on charge storage in a dielectric which forms part of the gate of an insulated gate field effect transistor. Feasibility has been demonstrated for MNOS (metal–nitride–oxide–silicon) memory devices[1,2] MAS (metal–aluminum–oxide–silicon) memory devices[3], and a dual gate MNOS memory device[4]. Difficulties in controlling the electrical characteristics of the storage dielectrics and additional fabrication steps required to achieve on-the-chip decoding, have limited the realization of these approaches to undecoded memory arrays of up to 256 memory bits.

Recently, feasibility of the ovonic amorphous semiconductor memory device has been demonstrated by fabrictaion of an undecoded 256 bit memory array[5].

The recent introduction[6] of a novel semiconductor memory element—, the FAMOS charge storage device, and its implementation in a fully decoded 2048 bit electrically programmable ROM[7], constitutes a significant advance in the state of the art of non-volatile semiconductor memories. It is the first available large capacity programmable ROM in which the information pattern is recorded electrically by way of a reversible change in memory device characteristics.

The Floating gate Avalanche injection MOS (FAMOS) memory device is essentially a *p*-channel silicon gate MOS insulated gate field effect device in which no electrical contact is made to the silicon gate. Operation of the FAMOS memory structure depends on charge transport to the floating gate by avalanche injection of electrons from either the source or drain *p–n* junctions.

The concept of an insulated gate field effect transistor with a floating gate as a non-volatile memory element was first advanced by Kahng and Sze[8]. Operation of the proposed structure was based on charge transport from the silicon substrate across a thin insulator layer ($\sim$ 50 Å) to a floating metal electrode which is covered by a second insulator and an upper metal gate. Charge is stored in the floating metal gate in response to an applied voltage between the upper metal and the substrate. The charge transport mechanism

involves tunneling of electrons from the substrate through the thin oxide to the floating metal gate. The formation of a metal gate over a very thin dielectric layer is the major obstacle in practical realization of this proposed structure. The same concept evolved to the MNOS structure in which the floating metal gate was replaced by a layer of traps in the silicon nitride.

Nicollian *et al.*[9], reported that high current densities can be achieved in MOS capacitors by avalanche injection of electrons from a *p*-type silicon substrate. They observed a considerably lower current density level due to hole injection from an *n*-type substrate.

The FAMOS memory structure investigated in the present work combines the floating gate concept with avalanche injection of electrons to yield a new nonvolatile memory element.

DEVICE STRUCTURE AND CHARACTERISTICS

A cross-section of the Floating gate Avalanche injection MOS (FAMOS) structure is shown in Fig. 1. It is a *p*-channel silicon gate MOS insulated gate field effect device (made on 5–8 Ω cm *n*-type material of ⟨111⟩ orientation), in which no electrical contact is made to the silicon gate. The floating gate is formed by deposition of a poly-silicon layer over 1000 Å of thermal oxide and is isolated from the top surface by 1·0 μm of vapor deposited oxide. The FAMOS memory structure depends on charge transport to the floating gate by avalanche injection of electrons from a *p*–*n* junction. A junction voltage in excess of −30 V applied to a *p*-channel FAMOS device will result in the onset of injection of high energy electrons from the *p*–*n* junction surface avalanche region to the floating silicon gate. Since the silicon gate is floating, the electron current through the oxide results in the accumulation of a negative charge on the gate. For a *p*-channel FAMOS device this negative charge will induce a conductive inversion layer connecting source and drain. The amount of charge transferred to the floating gate is a function of the amplitude and duration of the applied junction voltage. Once the applied junction voltage is removed, no discharge path is available for the accumulated electrons since the gate is surrounded by SiO_2, which is a very low conductivity dielectric. The accumulated negative charge on the gate will result in a change of device turn on voltage given by

$$\Delta V_T = -\left(\frac{Q_{G'} - Q_{G'}(0)}{C_0}\right)$$

where $Q_{G'}$ is the charge per unit area transferred to the floating gate, $Q_{G'}(0)$ is the initial charge on the floating gate, $C_0 = \epsilon_0 Ko/Xo$ is the capacitance per unit area of the thermal oxide layer, ϵ_0 is the permitivity of free space, Ko is the relative dielectric constant of silicon dioxide and Xo is the thermal oxide layer thickness.

Device turn on voltage V_T is given by

$$V_T = V_{FB} + 2\phi_F - \frac{Q_B}{C_0} - \frac{Q_{G'}(0)}{C_0}$$

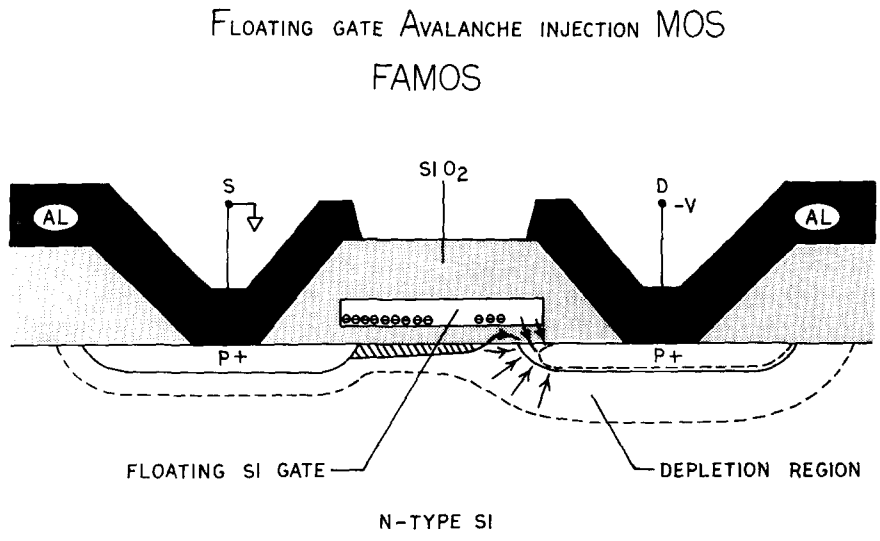

Fig. 1. Cross-section of FAMOS device under bias.

where Q_B is the charge within the substrate surface depletion region,

$$V_{FB} = \phi_{SS} - \frac{Q_{SS}}{C_0}$$

is the flat-band voltage, ϕ_{SS} is the polysilicon-silicon work function difference, Q_{SS} is the fixed charge at the silicon-silicon dioxide interface, and ϕ_F is the Fermi potential of the silicon substrate.

The presence or absence of charge on the floating gate can be sensed by measuring the conductance between the source and drain regions. The I_D-V_D characteristics of a charged and uncharged FAMOS device are shown in Fig. 2. Note that the uncharged FAMOS device conducts current for $V_D > -8{\cdot}0$ V even though no charge was transferred to the floating gate. The current is due to capacitive voltage feedthrough from the drain terminal to the floating gate. An illustration of the interelectrode capacitances in the FAMOS structure is shown in Fig. 3. If a negative voltage is applied to the drain of the device with the source and substrate at ground potential, a negative charge will be capacitively coupled to the floating gate by means of a displacement current through $C_{g'd}$ (Fig. 3(b)). The value of the corresponding negative feedback voltage $V_{G'f}$ is given by

$$V_{G'f} = V_D \frac{C_{g'd}}{C_{g'd} + C_{g's} + C_{g'b}}$$

where $C_{g'b}$ is the series combination of $C_{g'}$ and C_b (Fig. 3(b)). Once this capacitively coupled voltage to the floating gate exceeds the turn on voltage V_T, a conductive path is established between source and drain resulting in the onset of current flow. The same capacitively coupled voltage is responsible for the deviation of the charged FAMOS device I-V characteristic (Fig. 2) from that of an MOS transistor with the same geometry and an applied gate voltage equivalent to the amount of charge on the floating gate of the FAMOS device.

To account for the capacitive feedback effect, the amount of voltage capacitively coupled to the floating gate was measured as a function of applied drain voltage under two limiting conditions, $V_{G'} = Q_{G'}/C_0 = 0$ which corresponds to no electronic charge on the floating gate, and $V_{G'} > V_D$ which defines a charging condition of the gate resulting in complete inversion between source and drain without pinch-off. The feedback voltage value $V_{G'f}$ was obtained by measuring the drain to source current flow for a given drain voltage on the FAMOS device and determining the equivalent

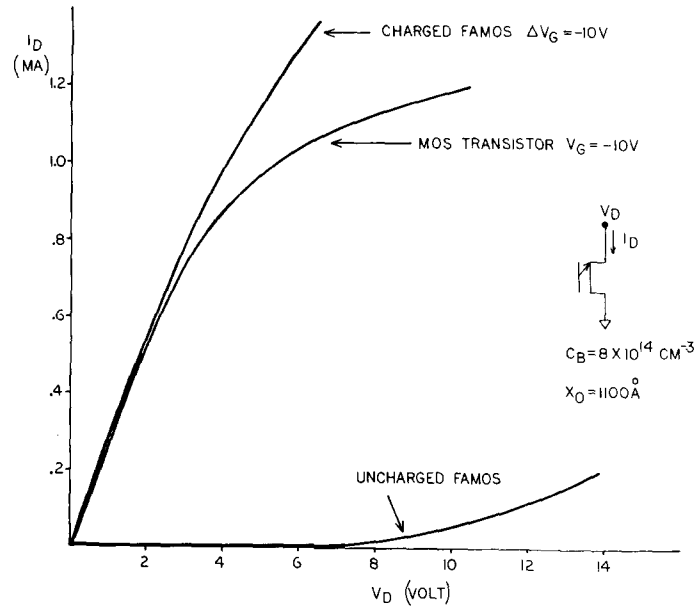

Fig. 2. I_D-V_D characteristics of charged and uncharged FAMOS device and the MOS transistor characteristic with a gate voltage corresponding to the amount of charge on the floating gate of the charged FAMOS device.

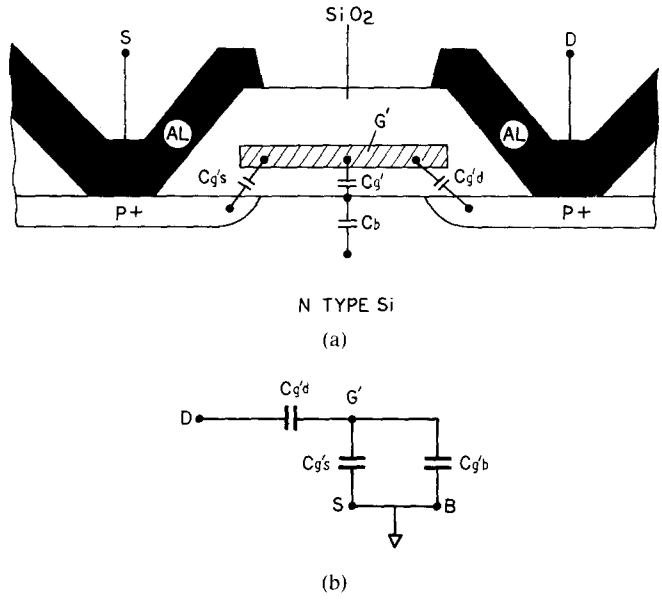

Fig. 3. (a) Cross-sectional view of the capacitances associated with the FAMOS structure. (b) Circuit representation of interelectrode capacitances.

gate voltage by comparison to an identical (process and geometry) MOS transistor. The two feedback voltage plots are shown in Fig. 4. The range of feedback factors $\Delta V_{G'f}/\Delta V_D$ stems from the variation of interelectrode capacitances as a function of drain voltage. For the $V_{G'} > V_D$ shown in Fig. 5(a), the induced inversion layer extends from source to drain and the gate capacitance $C_{g'}$ splits approximately evenly between $C_{g's}$ and $C_{g'd}$ which is reflected in a high feedback factor $\Delta V_{G'f}/\Delta V_D = 0{\cdot}45$. The condition $V_{G'} > V_D$ was obtained by charging the FAMOS device to a maximum $V_{G'}$-value of $-22{\cdot}0$ V. In the case of $V_{G'} = 0$ (Fig. 5(b)) when the feedback voltage $V_{G'}$ is greater than the turn on voltage V_T, the FAMOS device I_D–V_D characteristic corresponds to that of an MOS transistor in saturation. The capacitance $C_{g'}$ will be partially diverted to the source ($C_{g's}$) through the pinched off inversion layer. The capacitance $C_{g'd}$ consists of a combination of the floating gate to drain overlap capacitance in parallel with the capacitive feedback through the pinched off surface depletion region C_{dep} (Fig. 5(b)). The linearity of the feedback plot for $V_{G'} > V_D$ is due to the presence of a continuous conductive path between source and drain such that the ratio of $C_{g'd}/C_{g's}$ is independent of V_D.

On the other hand, the reason for the apparent linearity of the $V_{G'} = 0$ plot over the measured range of V_D is more involved. While an increase

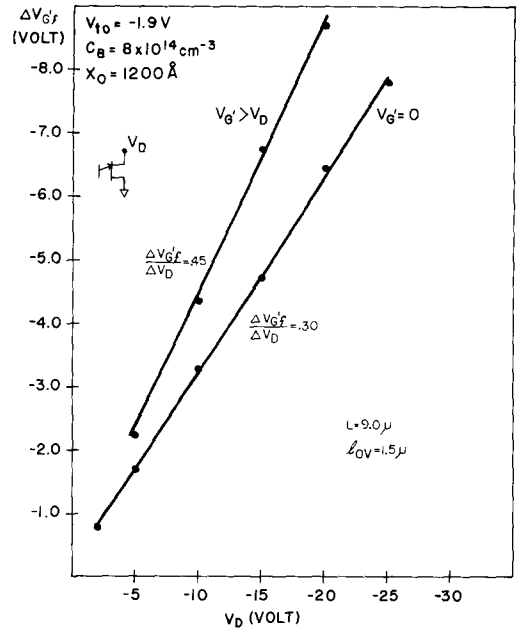

Fig. 4. Voltage feedback to the floating gate as a function of applied drain voltage.

in drain voltage is expected to increase the value of l_{dep} and thus affect the ratio of $C_{dep} + C_{g'd}/C_{g's}$ this tendency is countered by the effect of the electrical field in the oxide on l_{dep}[10]. This electric

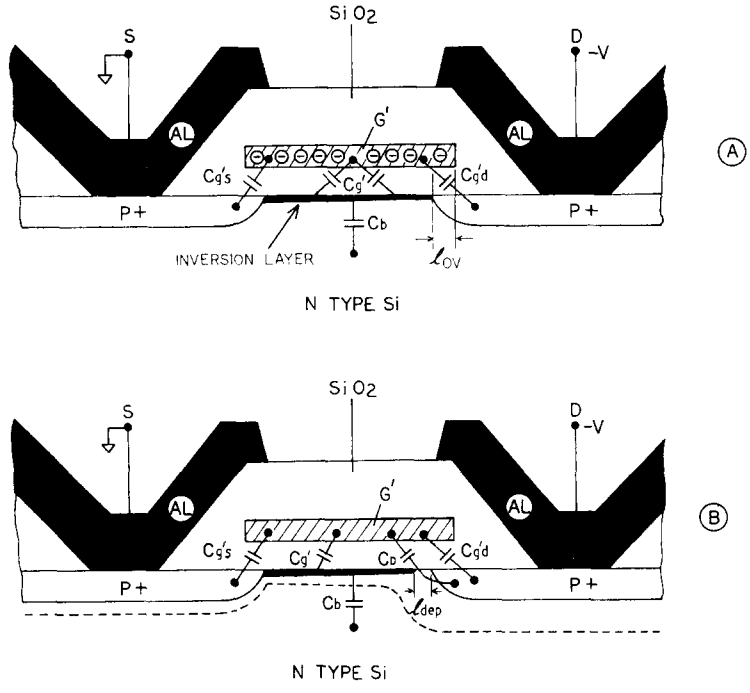

Fig. 5. Illustration of interelectrode capacitances for: (a) $V_{G'} > V_D$, (b) $V_{G'} = 0$.

field is a function of the potential difference $V_D - V_{G'}$ and tends to reduce the value of l_{dep} for increasing values of V_D. Hence the linearity of the $V_{G'} = 0$ plot can be traced to the opposing effect of the lateral field in the silicon and the vertical field in the oxide on the value of the drain surface depletion length l_{dep}.

Because of the pronounced effect of the feedback capacitance on device I_D–V_D characteristics it is expected to play an important role in the charging behavior.

DEVICE OPERATION

Consider the FAMOS device cross section shown in Fig. 1. Initially all terminals are at a common ground potential. The floating silicon gate is not charged and assumes the common reference potential. As the drain voltage is increased negatively with respect to the source and substrate, a positive potential drop appears across the overlap region between the floating gate and the p^+ drain diffusion. This increasing positive voltage will tend to invert the heavily doped p^+ drain region; however, because of the lack of supply of minority carriers (due to the reverse biased condition of the drain p–n junction) deep depletion will take place at the p^+ surface region of the drain near the SiO_2 interface. As the negative voltage on the drain is increased further the electric field in the induced surface depletion region will reach a value at which an avalanche multiplication condition is established. Some of the high energy electrons generated in the avalanching surface depletion region acquire a sufficient energy to surmount the Si–SiO_2 energy barrier and be swept by the electric field in the SiO_2 toward the conductive floating silicon gate.

The avalanche injection process is illustrated in Fig. 6 in terms of the variation of the energy bands with distance in a direction normal to the p^+ drain region. Initially (Fig. 6(a)) the structure is in equilibrium. The applied negative voltage (Fig. 6(b)) results in impact ionization and emission of electrons from the p^+ surface depletion region over the Si–SiO_2 energy barrier to the floating silicon gate. Finally (Fig. 6(c)) when the applied voltage is removed, the electrons are trapped in a potential well, bounded by polysilicon–silicon dioxide energy barriers on both sides.

(a) *Charge accumulation*

A detailed investigation of avalanche injection in response to an applied voltage pulse to metal–oxide–silicon (MOS) capacitor structures was performed by Nicollian *et al.* [11].

The current densities observed for hot electron

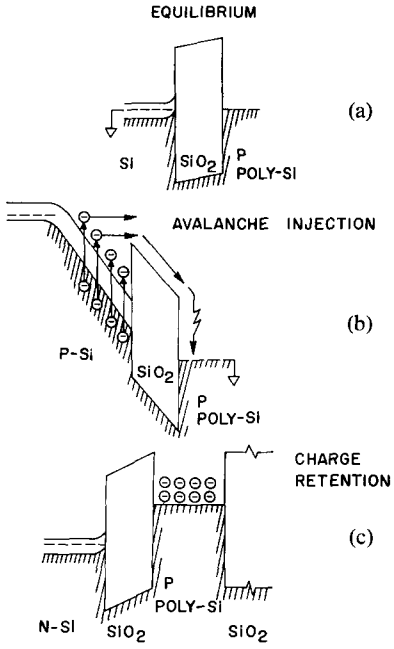

Fig. 6. Variation of the energy bands with distance in a direction normal to the p^+ drain region for a FAMOS device, (a) in equilibrium, (b) under avalanche injection, (c) after voltage removal.

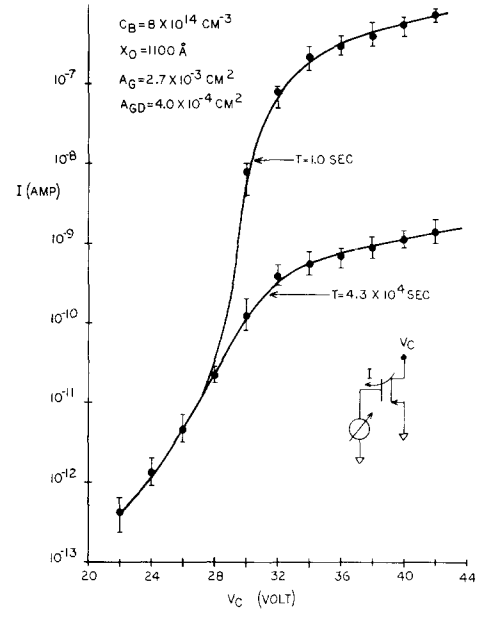

Fig. 7. Gate current as a function of applied drain voltage in an MOS transistor operating in the avalanche injection mode, for two values of applied voltage duration.

emission through the SiO_2 layer of an MOS capacitor made on a p-type substrate were of the order of 10^{-4} A/cm^2 at an oxide field of $3{\cdot}0 \times 10^6$ V/cm. Considerably lower current density levels were observed for hole injection from an n-type substrate.

Measurements of current flow through the oxide of a silicon gate MOS transistor operated in the avalanche injection mode (Fig. 7) indicate that charge transport in the FAMOS structure can be attributed to the same hot electron emission mechanism observed in MOS capacitors. The current density data in Fig. 7 are comparable to those reported by Nicollian *et al.*[9] for a given field in the oxide. An exact comparison between the data is complicated by the gradual surface carrier concentration profile along the surface of the p^+ drain region. The two distinct plots in Fig. 7 correspond to the initial and saturation values of current density through the oxide. As pointed out by Poirier and Olivier[12], when the avalanche injection current is measured, a potential drift is observed which corresponds to trapping of negative charge in the oxide. As a result, for a given d.c. applied voltage, the electric field distribution in the oxide is time dependent, leading to different initial and saturation values of current density. The rapid increase in current density and the gradual saturation is due to avalanche multiplication followed by an avalanche breakdown condition. In the carrier multiplication region, an increase in applied voltage enhances the electric field in the surface depletion region which leads to an increase in the number of hot electrons injected over the Si–SiO_2 barrier to the silicon gate. When the surface field reaches the critical value for the onset of avalanche breakdown, any further increase in applied voltage is dropped across the thermal oxide, resulting in the saturation of current density. If under the same experimental conditions (Fig. 7) the silicon gate is floating, the avalanche injected current results in the accumulation of a negative electron charge on the gate. The amount of charge transferred to the floating gate as a function of the applied junction voltage pulse amplitude and width is shown in Fig. 8. To verify that the charging effect is due to electron storage on the silicon gate and not due to trapping in the oxide at either interface, the charging experiments were repeated with a conventional silicon gate MOS transistor in which the metal connecting to the gate was left floating. The charging behavior was identical to that of the FAMOS device, and the stored charge could be removed by connecting the gate to ground. A

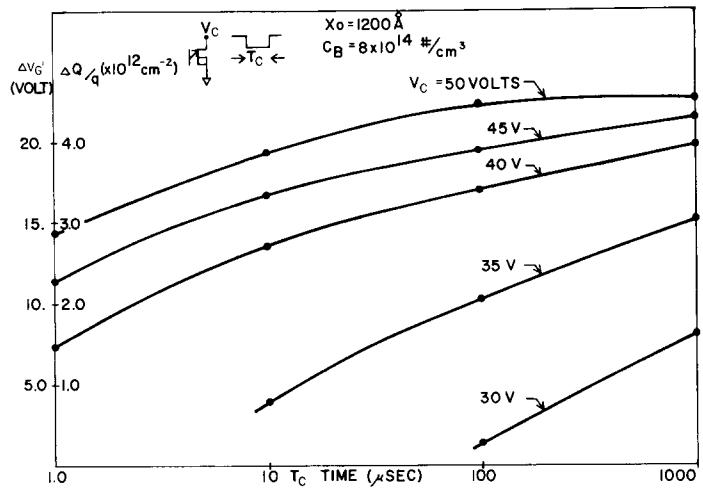

Fig. 8. Charge transferred to the floating gate of a FAMOS device as a function of applied charging voltage durations for different amplitudes of the applied voltage.

small residual charge of less than 10 per cent of the total accumulated charge was observed and attributed to trapping in the oxide[9,12]. The nature of this negative charge trapping will be interpreted further in the discussion of charge retention in the FAMOS structure. An attempt to correlate the current density date (Fig. 7) with the charge accumulated for a given applied voltage (Fig. 8) becomes difficult because of the different electric field distribution in the drain region of the MOS transistor and the FAMOS device. This difference in field distribution is caused by both the negative charge accumulation and capacitive feedback from the drain to the floating gate (detailed in the previous section). Both of these effects will reduce the potential difference between the floating gate and the drain, causing a decrease in the avalanche injected current with time. An accurate numerical account of these effects requires detailed knowledge of the time dependent field distribution in the deep depleted p^+ surface depletion region.

An additional effect not reflected in the current measurements in Fig. 7 is due to enhancement of carrier multiplication in the pinch off region of the FAMOS device by injection of carriers from the inversion layer. Such an enhancement of carrier mulitplication affecting drain junction breakdown in an MOS transistor has been previously reported [13]. As shown in Fig. 9, gate current measurements under the condition $|V_G| > |V_T|$ (on the MOS transistor used in Fig. 7) indicate an increase of avalanche injection current which can be attributed to onset of current flow. An increase in

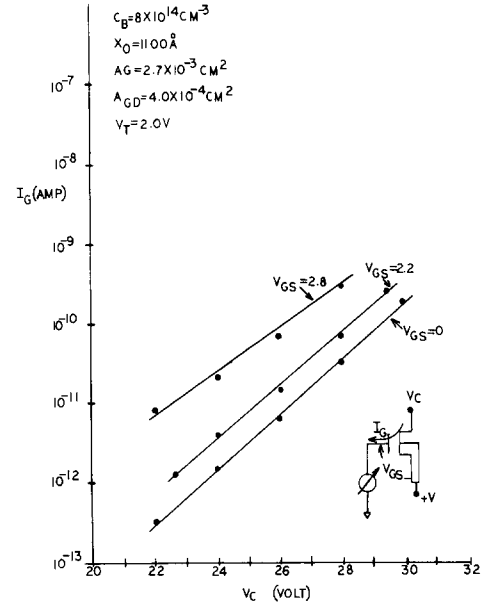

Fig. 9. Gate current as a function of applied drain voltage in an MOS transistor operating in the avalanche injection mode, for different values of gate to source voltage.

gate voltage to simulate current flow conditions during charging of the FAMOS device would lead to excessive currents through the MOS transistor because of the large gate area required to record the low level gate current.

Another aspect of interest concerning the charge accumulation data is the existence of a charging threshold. The value of this threshold was obtained from a measurement of charge saturation

as a function of applied charging voltage to the drain. Saturation was defined as charge accumulation after 12 hr of applied voltage. The results are shown in Fig. 10. From knowledge of the amount of charge accumulation and the feedback voltage to the gate (measured by the same method discussed with reference to Fig. 4), the saturation gate to drain voltage was determined as a function of applied voltage as shown in Fig. 11. The results indicate that saturation of charge transfer occurs at a constant gate to drain voltage of 8·0–9·0 V independent of the applied charging voltage. This value is within measurement error of the charging threshold voltage extrapolated from Fig. 10. The low charging threshold points to the possibility

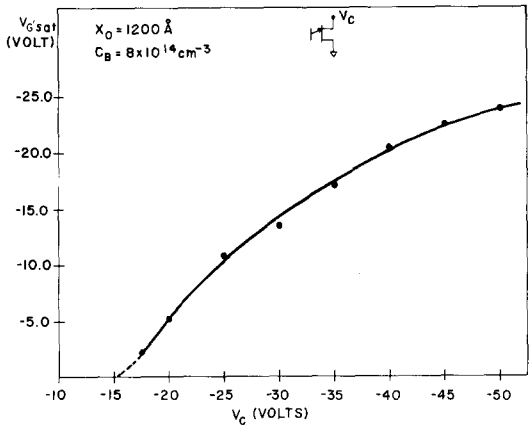

Fig. 10. The amount of charge transferred to the floating gate as a function of the steady state applied charging voltage.

that initial charging takes place by way of thermally generated electrons from the reverse biased surface depletion region.

(b) *Charge retention*

Once the applied charging voltage is removed, no discharge path is available for the accumulated electrons, since the gate is surrounded by thermal oxide which is a very low conductivity dielectric. The electric field in the structure after the removal of junction voltage is due only to the accumulated electron charge and is not sufficient to cause appreciable charge transport across the poly-silicon–thermal oxide energy barrier. The maximum stored charge of 4×10^{12} No./cm^2 ($V_W = 50$ V, Fig. 8) results in an electric field of approximately 2×10^6 V/cm across the thermal oxide. Assuming current transport by Fowler–Nordheim emission from the poly-silicon gate into the oxide[14], the estimated discharge current (for a polysilicon–SiO_2 energy barrier of at least 3·2 eV) is of the order of 10^{-40} A/cm^2 at 300°K. Charge decay plots as a function of time for different initial charge values at 125 and 300°C are shown in Fig. 12. The rapid initial decay followed by a logarithmic time dependence cannot be explained by electron transport across the oxide. It has been shown[15,16] that an MOS structure subjected to a high electric field in the oxide by means of a negative bias applied to the gate at elevated temperature exhibits positive charge accumulation at the Si–SiO_2 interface. A charged FAMOS device incorporates the negative bias in the form of a negatively charged gate. Hence, one would

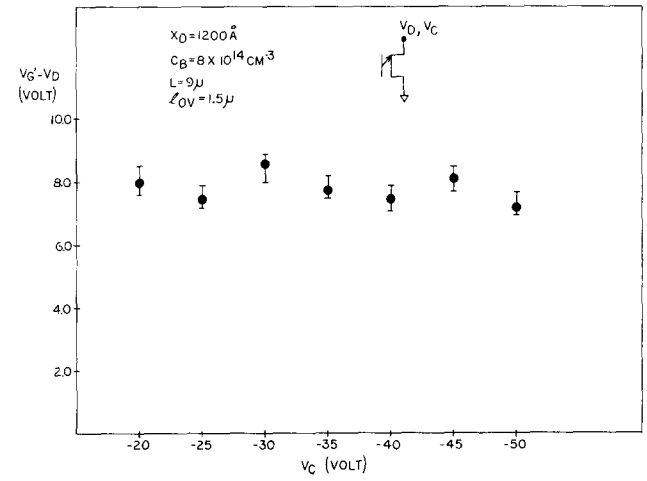

Fig. 11. Floating gate to drain potential difference as a function of the steady state applied charging voltage.

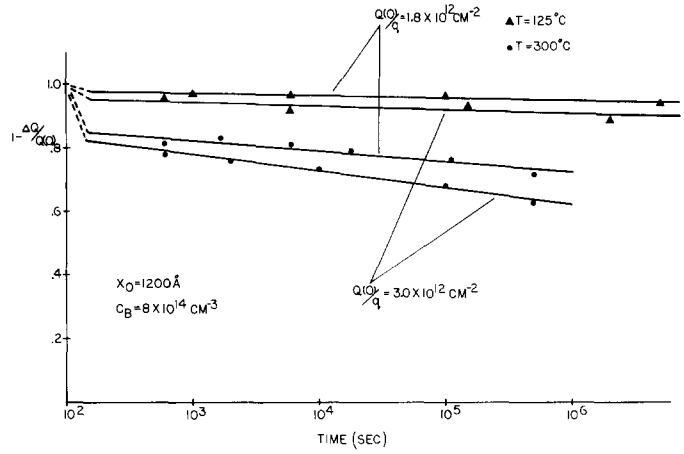

Fig. 12. Retention of stored charge as a function of time at 125 and 300°C for two values of initial charge accumulation on the floating gate.

expect positive charge accumulation to take place at the Si interface during storage at elevated temperatures. To verify that the temperature and electric field dependence of the logarithmic portion of charge decay (Fig. 12) in a FAMOS device can be attributed to positive charge accumulation, these data were compared with the turn on voltage shift for an identically processed MOS transistor subjected to an electric field equivalent to the amount of charge stored on the FAMOS device. The results shown in Fig. 13 indicate identical logarithmic behavior for the two structures. The activation energy of positive charge build-up was measured to be 1·0 eV, which agrees well with previously published data[16]. The discrepancy in the magnitude of charge build-up

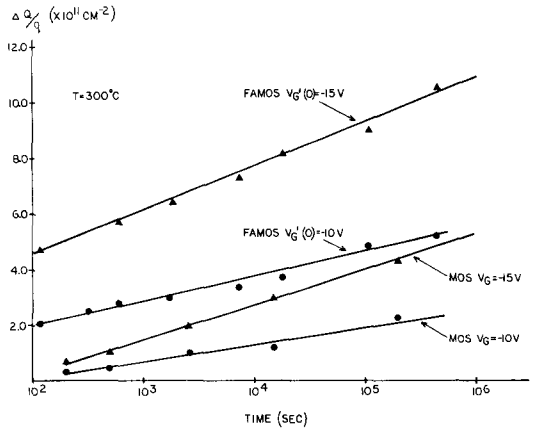

Fig. 13. Comparison of positive charge accumulation at the Si–SiO_2 interface under negative bias at 300°C, with charge loss in a FAMOS device stored at 300°C.

in the two structures (Fig. 13) is due to the rapid initial charge decay in the FAMOS structure which exhibits different field and temperature characteristics from that of the logarithmic portion. This feature can be related to charge removal by thermal excitation of electrons from shallow traps in the oxide. It was pointed out in the description of avalanche current measurements in an MOS structure (section 2(a)) that the nature of the current characteristics in Fig. 7 is a result of negative charge trapping in the oxide. The characteristics of trapped charge can be derived from gate current measurements on an MOS transistor operating in the avalanche injection mode. The family of I–V plots shown in Fig. 14 corresponds to gate current measurements after application of different values of steady state (12 hr) voltage to the drain of an MOS transistor.

The applied drain voltage was increased in 2·0 V increments and the current recorded after 12 hr, resulting in the leftmost steady state I–V characteristic. After steady state had been reached at a given voltage, gate current measurements were repeated at lower applied voltages to detect any changes in current flow. The family of I–V characteristics represents the reduction in current flow due to charge trapped in the oxide during application of the steady state voltage. Each of the characteristics was obtained on a different transistor from the same processed wafer.

The parallel nature of the resulting I–V characteristics suggests that the reduction in current could be interpreted as a decrease in the voltage dropped across the drain (p^+) surface depletion region. This voltage shift reflects the amount of

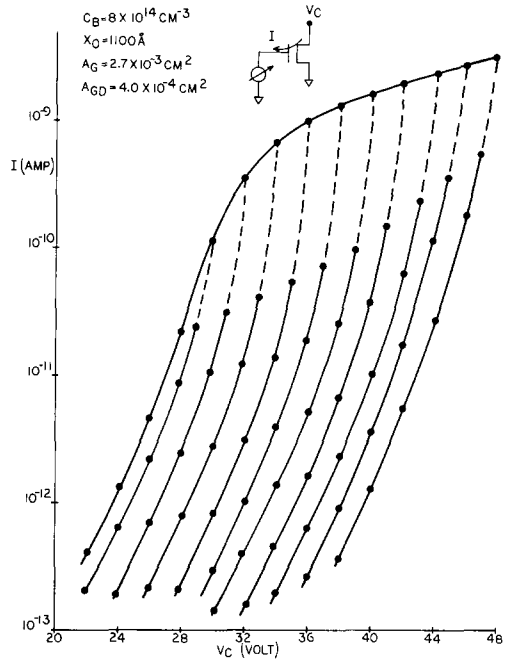

Fig. 14. Hysteresis behavior of gate current as a function of applied drain voltage in an MOS transistor operating in the avalanche injection mode. A_{GD} is the gate to drain overlap area.

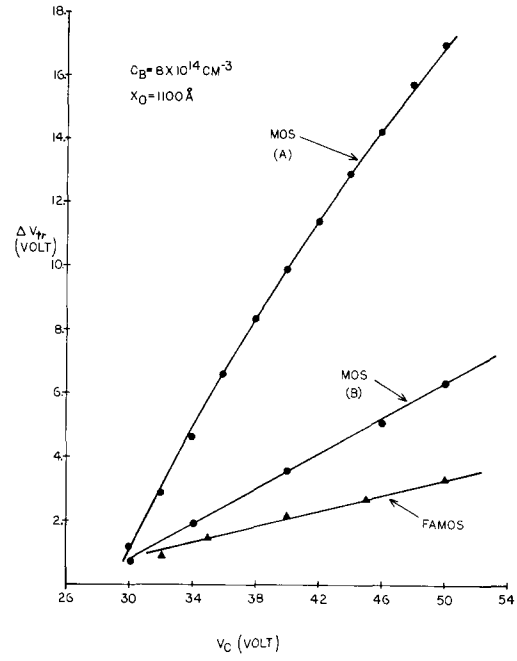

Fig. 15. Charge trapping in an MOS transistor operated in the avalanche injection mode, (a) before high temperature storage, (b) after 60 sec storage at 300°C. Initial charge loss of a FAMOS device stored 60 sec at 300°C is shown for comparison.

charge trapped and is plotted as a function of the steady state applied voltage V_C in Fig. 15. The ΔV_{tr}-values were obtained by determining the amount of voltage offset for each of the I–V plots in Fig. 14 with respect to the (leftmost) steady state I–V characteristic.

To evaluate the effect of high temperature storage on the trapped charge, the experiments leading to the I–V plots in Fig. 14 were repeated with the following modification. After steady state was reached at a given applied voltage, the device was heated without bias for 60 sec at 300°C. The voltage shift ΔV_{tr} of the I–V characteristics measured after storage is plotted as a function of steady state voltage V_C in Fig. 15(b). The lower values of ΔV_{tr} for a given V_C compared to plot A indicate a substantial loss of trapped charge during high temperature storage.

For qualitative comparison, the initial charge loss in a FAMOS device (as a function of the applied charging voltage) after 60 sec of storage at 300°C, is also plotted in Fig. 15. While the voltage and temperature dependence of both charge loss mechanisms is similar, the magnitudes are considerably different. If one assumes that the trapped charge is a function of the avalanche injected current density, the magnitude of trapped charge in the FAMOS structure should be small compared to that of the MOS structure because of the lower gate to drain voltage drop for a given applied drain voltage (section 2(a)). However, a quantitative correlation between the charge loss mechanisms in both structures requires detailed knowledge of the field distribution in the avalanche injection region.

(c) *Charge removal*

To provide a useful memory function, it is desirable to be able to remove the charge from the floating gate. Since the gate is not electrically accessible, charge removal by means of an electrical pulse becomes difficult. The possibility of compensating the electron charge by injection of holes from the substrate is questionable due to the lack of evidence for substantial hole conduction through the oxide. However, the initial equilibrium condition of no electronic charge on the gate can be restored by illuminating the device with ultraviolet light or by exposure to X-ray radiation. The two charge removal processes are illustrated qualitatively in Fig. 16. Illumination with ultraviolet light (Fig. 16(a)) of the appropriate

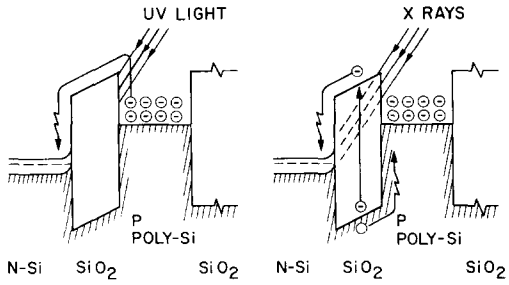

Fig. 16. Illustrations of charge removal by ultraviolet light and X-ray irradiation.

wavelength will impart sufficient photon energy to the stored electrons to excite them over the barrier with the aid of the built-in field in the oxide to the silicon substrate. If we assume a degenerate p^+ polysilicon gate, the energy barrier faced by the electrons is approximately 4·3 eV. Hence, an ultraviolet wavelength corresponding to a photon energy in excess of 4·3 eV will result in a discharging photo current from the floating gate to the substrate. A typical charge removal plot for a FAMOS device obtained by exposure to 2537 Å (4·9 eV) ultraviolet light is shown in Fig. 17.

Charge removal by X-ray radiation (Fig. 16(b)) involves the generation of hole electron pairs in the oxide by the ionizing radiation which has an energy greater than the band gap of SiO_2 (approx. 8·0 eV). A plot of charge removal as a function of radiation dose is shown in Fig. 18. The radiation dose required for complete charge removal, 5×10^4 rads, is comparable to the dose reported by

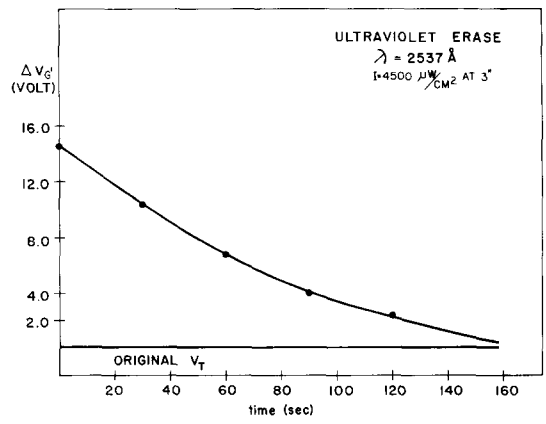

Fig. 17. The amount of charge removal by ultraviolet light as a function of time. I is the measured intensity of the light.

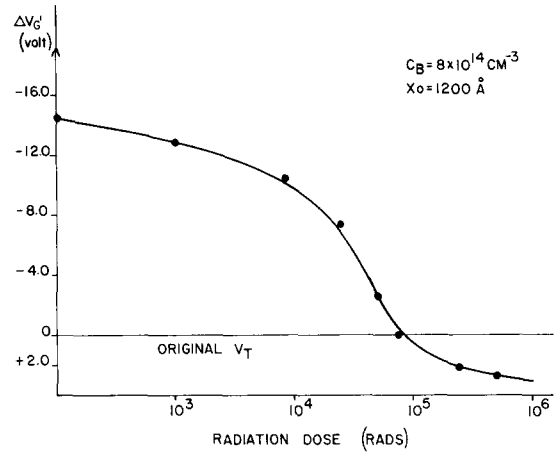

Fig. 18. Charge removal by X-ray irradiation as a function of radiation dose.

Snow *et al.* [17] for the onset of radiation induced turn on voltage shift in MOS transistors. As reported in the literature concerning the exposure of semiconductor devices to X-ray radiation, [17,18] the positive charge accumulation resulting from trapping in the oxide can be annealed at temperatures above 200°C. To evaluate the effect of exposure to ionizing radiation on the storage retention capability of the FAMOS device, the charge decay characteristics at 200°C were compared for irradiated (annealed at 200°C for 15 hr) and non-irradiated units charged to the same value. The results are shown in Fig. 19, and indicate that no significant difference in retention characteristics can be discerned.

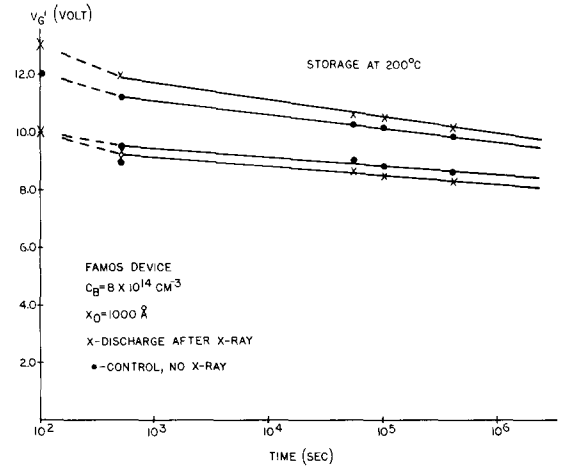

Fig. 19. Comparison of charge retention for irradiated FAMOS devices annealed 15 hr at 200°C with non-irradiated units.

DEVICE APPLICATIONS

A non-volatile charge storage device with long term retention and charge removal capability has many potential applications in the areas of digital and analog circuits. Semiconductor memories, photo-sensitive storage arrays, depletion mode load devices in digital circuits and analog storage circuits are a few specific examples. However, the most widespread potential application is in the area of semiconductor programmable read only memories. Fabrication of a monolithic 2048 bit fully decoded electrically programmable read only memory with FAMOS devices in the basic memory cell has been previously reported[7]. A photomicrograph of the integrated circuit memory chip is shown in Fig. 20. While most of the design aspects of the memory chip relate to circuit design techniques detailed in another publication[19], some of the considerations involving the memory cell deserve elaboration from a device standpoint. Two possible ways of incorporating a FAMOS device in a programmable read only memory cell are shown in Fig. 21. Since the storage device (T_1) is a two terminal device, an additional isolation MOS transistor (T_2) is required to avoid erroneous interpretation of information due to coupling between normally 'on' (charged) FAMOS devices in the memory array. In both schemes shown in Fig. 21, programming of the storage device is accomplished by a coincidence negative voltage applied to the X and Y select lines, resulting in avalanche injection and retention of charge on the floating gate of the storage device. Despite the apparent symmetry of the two schemes (Fig. 21) they differ in their programming characteristics. Configuration I (Fig. 21(a)) for the same T_2 device size results in a lower voltage at the drain terminal of the FAMOS device for a given programming voltage V_p due to the lower conductance of T_2 under this biasing configuration. Consequently, the amount of charge transferred to the floating gate for a given programming pulse amplitude and width is less for Configuration I compared with that of Configuration II.

Proper operation of the memory requires the capability to inhibit the programming of a non-selected bit. In Configuration I (Fig. 21(a)) this is simply accomplished by the lack of a Y-select signal or the absence of an X-select excitation, which inhibits the transfer of the programming pulse to the drain of the FAMOS device. On the other hand, in Configuration II (Fig. 21(b)) the inhibit mechanism in the case of no X-select signal is more complicated. If the X-select line is grounded while a negative voltage is present on the Y-select line, the drain of the FAMOS device (Fig. 21(b)) is still subjected to a high negative voltage, however, no avalanche injection will occur in this case because the source of the storage device is floating (T_2 is 'off'). The absence of avalanche injection can be understood with the aid of the capacitive feedback considerations discussed in Section I. Under the programming condition (T_2 'on') the capacitance distribution in the FAMOS device is similar to that illustrated in Fig. 5(b). The feedback factor $\Delta V_{G'f}/\Delta V_D$ is of the order of 0·3. Hence the value of $V_{G'f}$ for a typical drain voltage of -40 V during programming is -12 V. The potential difference $V_{G'} - V_D$ is substantially above the charging threshold shown in Fig. 11. However, if the source is floating (in the inhibit mode) the shunt capacitance to ground is very small since $C_{g's}$ through the negatively

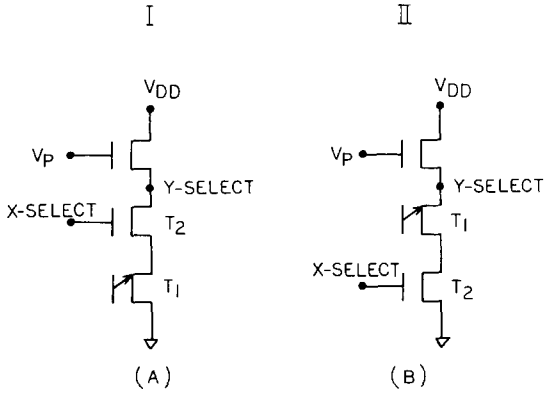

Fig. 21. Two configurations for incorporating FAMOS device in a programmable memory cell.

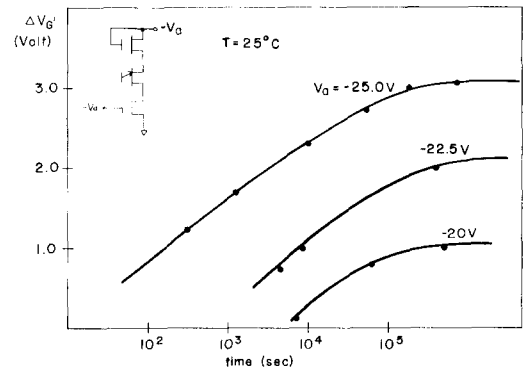

Fig. 22. Charge accumulation as a function of time in a memory cell for different values of applied READ voltage.

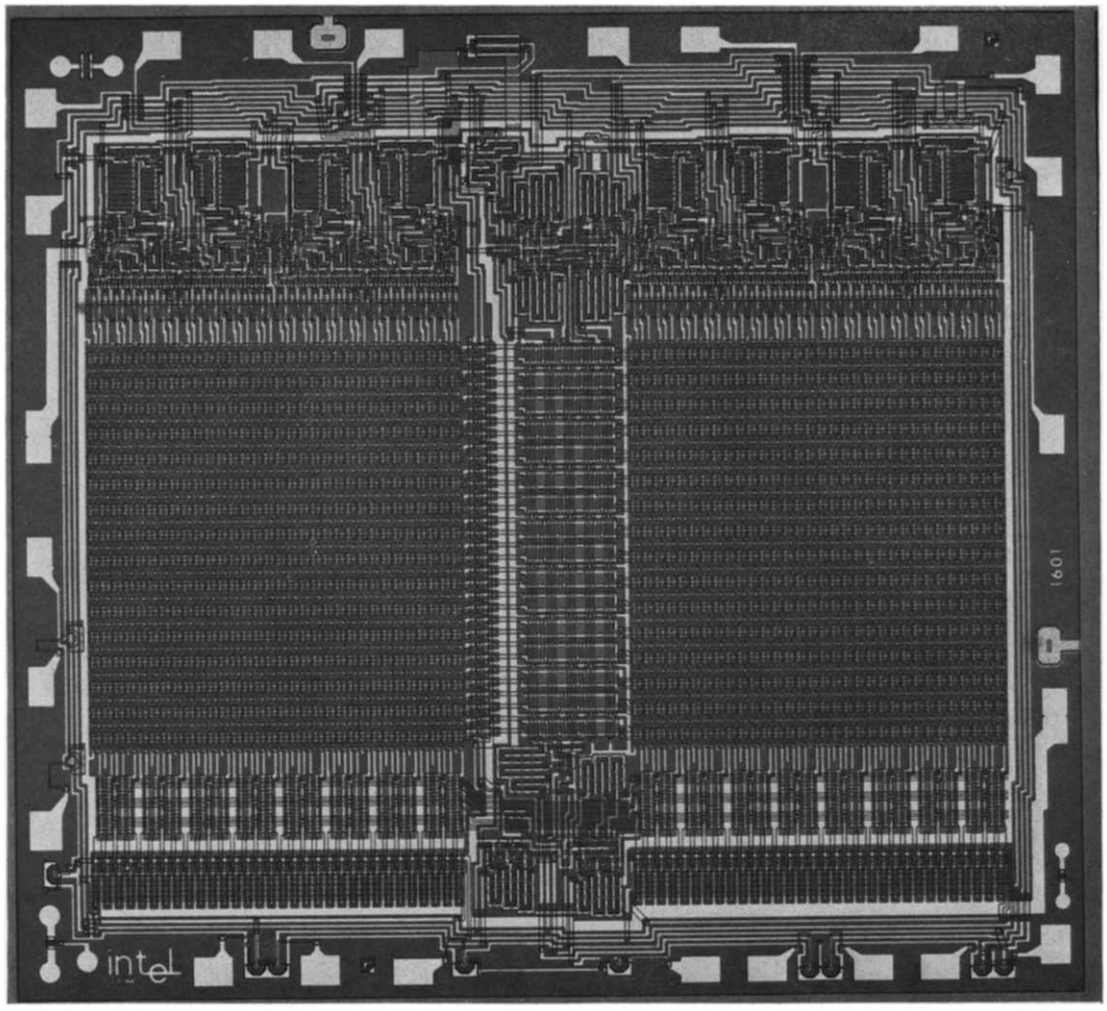

Fig. 20. Photomicrograph of a 2048 bit electrically programmable FAMOS read only memory.

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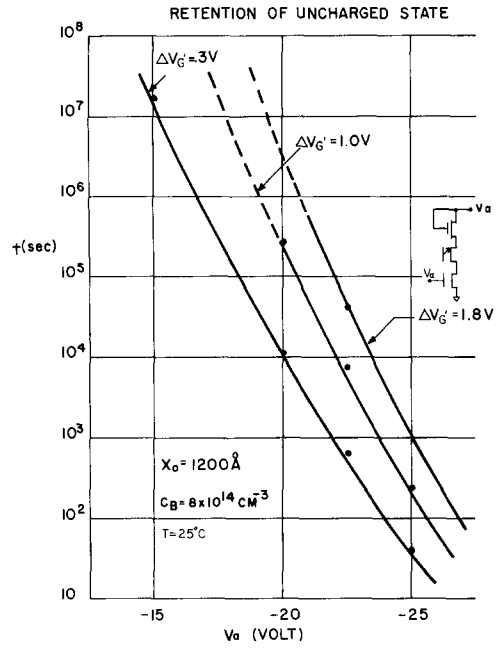

Fig. 23. Retention of the uncharged state in a memory cell as a function of the applied READ voltage.

rising voltage on the floating source provides additional feedback to the gate. As a result, the feedback factor can be as high as 0·8–0·9. $V_{G'} - V_D$ becomes smaller than the charging threshold and no avalanche injection occurs.

Once a memory cell has been programmed, it can be interrogated in the READ mode by coincidence selection (X, Y) with a lower negative voltage (-15 V). Hence the only difference between selection in the PROGRAM mode and the READ mode is the applied voltage level -50 and -15 V, respectively. This brings up the question of whether an uncharged memory cell can be slowly charged by repeated selection in the READ mode. The memory cell in configuration II (Fig. 21(b)) is particularly susceptible because of its advantage in programmability.

Parasitic charging in this configuration was measured for different voltages as a function of time. The results shown in Fig. 22 indicate charging characteristics followed by saturation similar to those shown in Fig. 8. Computation of the saturation value $V_{G'} - V_D$ yields 7·5 V for all three voltages, which is in good agreement with the saturation value obtained from Fig. 11. To estimate the long term effect of parasitic charging on the retention of the uncharged memory state under READ mode operating conditions ($V_a = -15$ V), the time dependence is plotted in Fig. 23 as a function of applied voltage for different values of parasitic charge accumulation. A voltage shift of $\Delta V_G = 1{\cdot}0$ V at $V_a = -15$ V will occur at an extrapolated time of at least 10 years. Hence parasitic charging does not present a practical reliability problem for memory cell operation.

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